THE DESIGN OF BROADBAND FREQUENCY DOUBLERS USING CHARGE-STORAGE DIODES*

by

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With varying degrees of approximation, the parametric action in many frequency multipliers can be viewed as the coupling of impedances at different frequencies by means of an impedance inverter. One such multiplier which can be so characterized is the charge-storage multiplier without idlers.[1] In the equivalent circuit for such a multiplier, as shown in Fig. 1, the time-varying action of the diode is represented by the impedance inverter marked K. The load impedance at the output frequency, Z_L, is transformed into the impedance Z_{in} at the input frequency according to the relation

$$Z_{in} = \frac{K^2}{Z_L} \tag{1}$$

At midband, $Z_L = R_s + R_L$, and we find that for optimum efficiency

$$\text{Efficiency} = \frac{\sqrt{1+N}-1}{\sqrt{1+N}+1} \tag{2}$$

$$R_g = R_L = R_s\sqrt{1+N} \tag{3}$$

$$R_{in} = \frac{K^2}{R_s+R_L} = R_s\sqrt{1+N} - R_s \tag{4}$$

where $N = \left(\frac{K}{R_s}\right)^2$, and R_s is the diode series resistance.

For the specific case of the charge-storage diode doubler, the impedance inverter constant is

$$K = \frac{2}{3\pi\omega C} \tag{5}$$

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NOTES

where ω is the angular input frequency, and C is the diode reverse bias capacitance (a constant for the idealized charge-storage diode).

When designing even-order, wideband multipliers, the most desirable configuration to use is a balanced one employing two diodes. Such a configuration will separate even from odd-order harmonics by the symmetry of the circuit. This approach results in comparatively simple circuits which are easily tuned and capable of the maximum possible bandwidth. When such a balanced circuit is used for a broadband doubler, up to an octave in bandwidth is possible before unwanted harmonics can occur within the passband of the output of the doubler (assuming perfect balance).

Shown in Fig. 2 is a sketch of the circuit used in the experimental doubler. The circuit is primarily of slab-line construction. At the input a two-step $\lambda/4$ transformer is used to transform 50Ω to 20Ω. At the end of the transformer is a short-circuited $\lambda/4$ stub which forms the first resonator and which can also serve as a DC return for the diodes. Also at the end of the transformer is a short section of high-impedance transmission line which connects the diodes to the input. This section of the circuit with the two diodes effectively in parallel, together with the balun, forms the second resonator (series resonant). The remaining three resonators of this five-resonator design are at the output frequency. The first output frequency resonator consists of the two diodes in series with the short section of line connecting them. The second output resonator is effectively a shunt resonator (actually two in parallel) formed by the short-circuited $\lambda/4$ balun arms. The final output resonator is an open-circuited $\lambda/4$ line in series with the output. This last resonator is physically located inside one of the balun arms as indicated in Fig. 3. Not only does this last resonator act as a further broadbanding resonator, but it also gives a required DC block. DC bias is supplied to the diodes through the balun arms, which are DC isolated. A lumped-circuit equivalent of the entire multiplier circuit is shown in Fig. 4.

A five-resonator doubler circuit of this type may be designed with the aid of conventional filter prototypes. Figure 5(a) shows a five-reactive element low-pass prototype filter[2] and Fig. 5(b) shows a simplified equivalent circuit for the corresponding frequency doubler. The parameters χ_2, χ_3, and χ_5 are reactance slope parameters and $\mathcal{b}_1$ and $\mathcal{b}_2$ are susceptance slope parameters defined by

$$\chi_k = \frac{\omega_0}{2} \left.\frac{dX_k}{d\omega}\right|_{\omega=\omega_0} \quad \text{and} \quad \ell_k = \frac{\omega_0}{2} \left.\frac{dB_k}{d\omega}\right|_{\omega=\omega_0} \tag{6}$$

where X_k is the reactance of series resonators, B_k is the susceptance of shunt resonators, and ω_0 is the resonant frequency. It is convenient in the circuit in Fig. 5(b) to refer to one diode alone, and since the diodes are in parallel for the input frequency, the impedance level of the actual input circuit should be doubled for analysis on a per-diode basis; while since the diodes are in series at the output frequency, the impedance level of the actual output circuit should be halved for analysis on a per-diode basis.

The parameters χ_2, χ_3, K, and R_s are fixed by the diode and its resonating circuit, and the remainder of the circuit must be designed around these parameters. Neglecting R_s, the remaining parameters for the design are given by

$$w = K\omega_1 \sqrt{\frac{g_2 g_2}{\chi_2 \chi_3}}, \qquad R_0 = \frac{\chi_2 w g_0}{\omega_1 g_2}$$

$$\ell_1 = \frac{\omega_1 g_1 g_0}{w R_0}, \qquad R_6 = \frac{\chi_3 w}{\omega_1 g_3 g_6}$$

$$\ell_4 = \frac{\omega_1 g_4}{w R_6 g_6}, \qquad \chi_5 = \frac{\omega_1 g_5 R_6 g_6}{w} \tag{7}$$

where w is the fractional bandwidth of the doubler. If R_s is small, conventional low-pass prototypes can be used with good results. However, for larger values of R_s, prototypes which involve resistive loading of elements g_2 and g_3 should be used. In the above equations K is assumed to be evaluated at the midband frequency. Since K actually varies with frequency, the response will be distorted. However, our computer studies show that this distortion can be corrected very nicely by stagger tuning the resonators so that resonators ℓ_1, ℓ_4, and χ_5 are tuned a certain percent low, while resonators χ_2 and χ_3 are tuned a certain percent high (the percent to be used depends on the bandwidth).

Before the experimental multiplier was tested on a large-signal basis, all of the resonators were pretuned under small-signal conditions. The resonators involving the diodes were

tuned with forward bias applied to the diodes to simulate the estimated average large-signal capacitance. When then tested under actual large-signal operation, very little retuning was required. Shown in Fig. 6 is a plot of the experimentally measured efficiency together with a computed curve. The computed curve is based upon experimentally measured resonator slope parameters, the theoretically predicted value for the inverter constant, and an empirically determined value of diode series resistance to yield a best fit to the midband efficiency. The agreement between theory and experiment is considered good. Note that the experimental results show an octave bandwidth at efficiencies of about 50%.

ACKNOWLEDGEMENT

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REFERENCES

1. R. H. Johnston and A. R. Boothroyd, "Charge storage frequency multipliers," Proc. IEEE, vol. 56, no. 2, pp. 167-176, February 1968.

2. G. L. Matthaei, L. Young, E.M.T. Jones, Microwave Filters, Impedance-Matching Networks, and Coupling Structures, McGraw-Hill Book Company, New York, 1964.

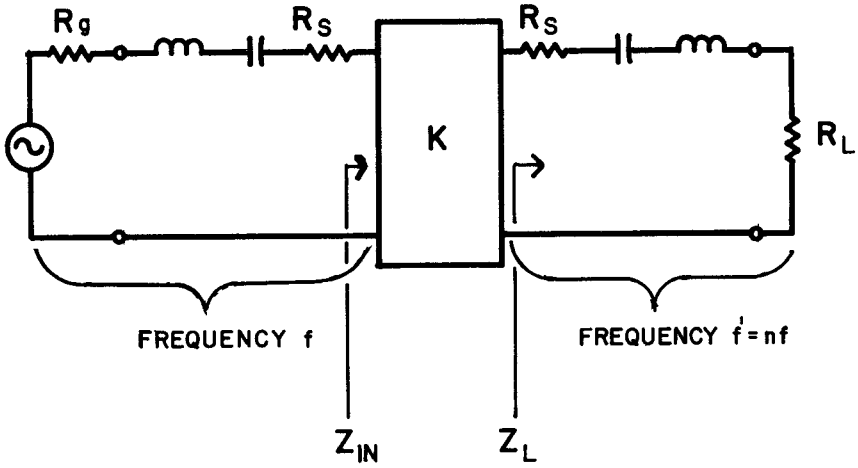

Figure 1 An equivalent circuit of a simple frequency multiplier with the time-varying portion of the capacitance represented by an impedance inverter.

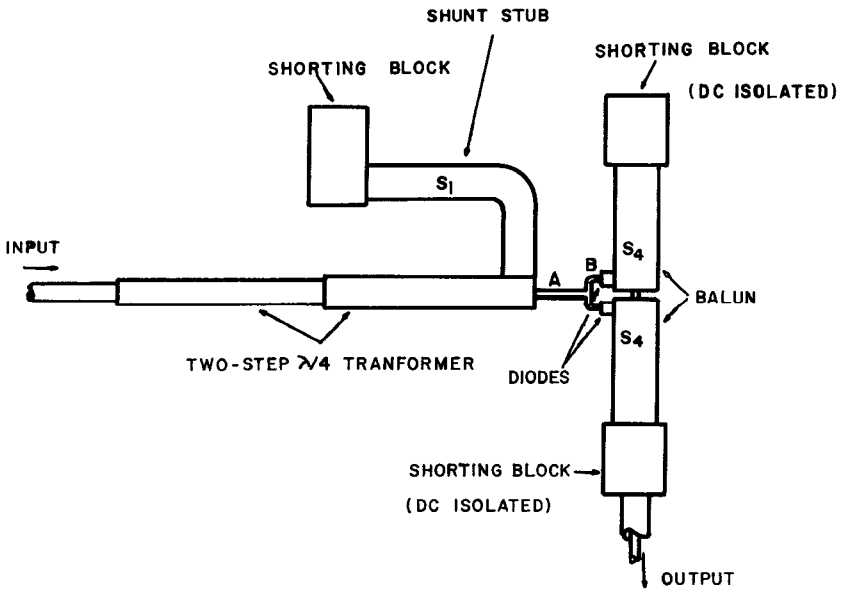

Figure 2 Circuit configuration of the experimental broadband doubler.

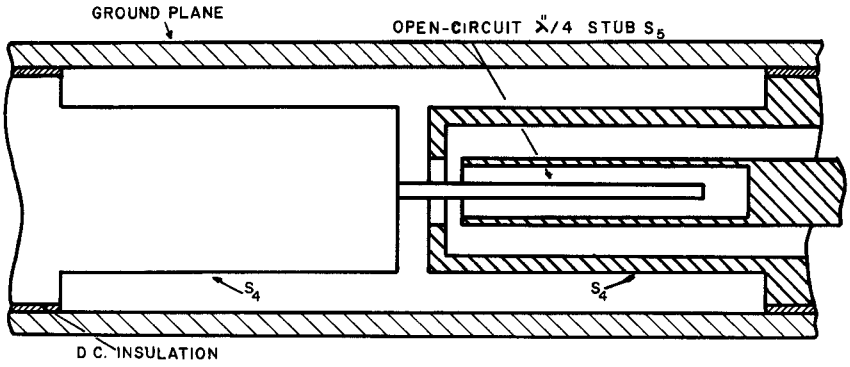

Figure 3 Cross-section of a doubler balun, showing construction of the final output resonator.

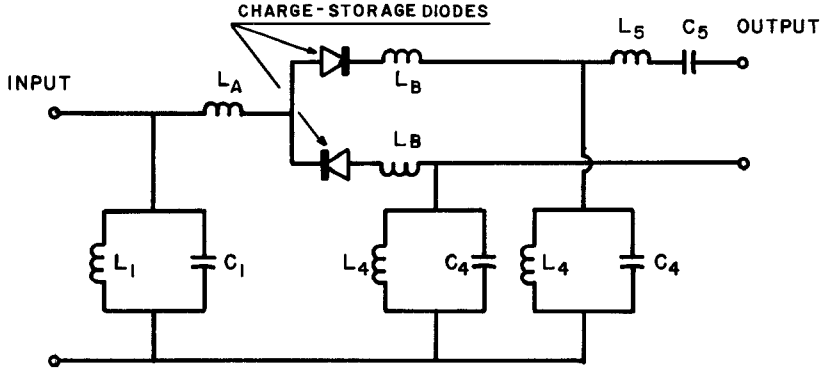

Figure 4 A lumped-circuit equivalent of the experimental broadband doubler.

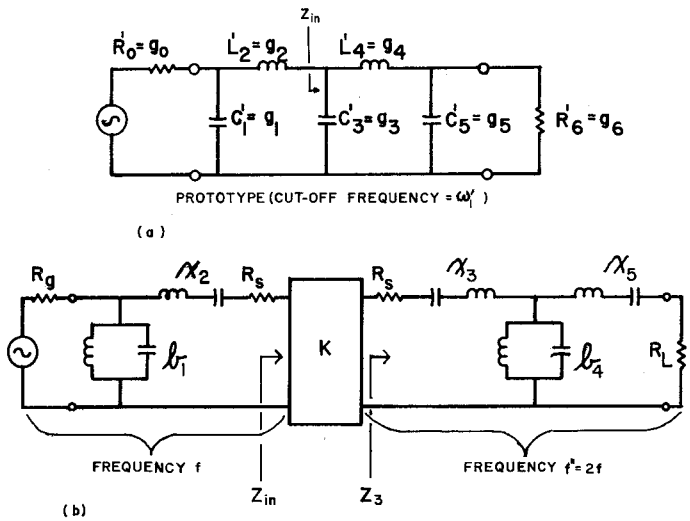

Figure 5 At (a) is shown a five reactive element low-pass prototype, and at (b) is shown the corresponding doubler equivalent circuit.

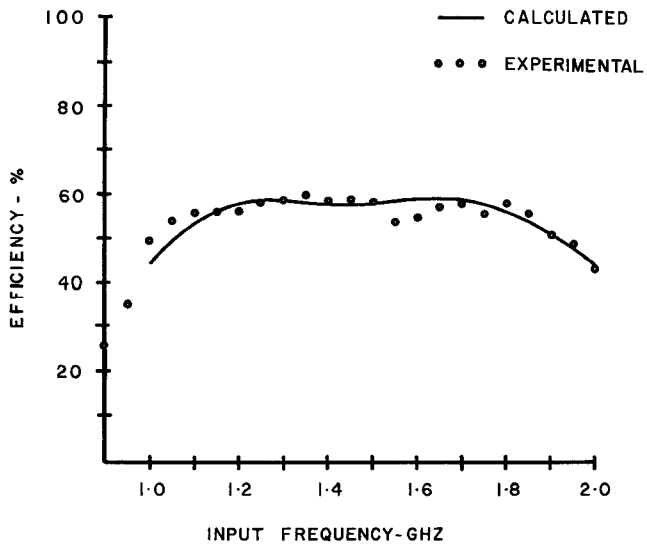

Figure 6. A comparison between theory and experiment for the broadband doubler.